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Analysis of hybrid topology for multilevel inverter to maximize the number of output voltage levels for PV-battery system[1]

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Abstract. In this paper, novel symmetric and asymmetric cascaded multilevel inverter topologies are proposed which are based on the developed H-bridge and half bridge inverter combination, semiconductor switches, the gate driver circuit numbers of which are reduced. Series connection would be beneficial bursting the excessive output levels and maximizing different levels generated by the inverter. For the proposed topology, two algorithms have been suggested to determine the magnitudes of DC voltage sources. The DC sources of presented structure are photovoltaic panels and battery. To determine the proposed topology performance, the inverter is implemented experimentally as a lab prototype.

Key words. PV-Battery, multilevel inverter, reduction of switches.

1. Introduction

Various multilevel inverter topologies of high voltage and high power applications have appeared during the recent years [1–3]. This is mainly due to the attractive advantages of multilevel inverters such as high quality output voltage production, lower total harmonic distortion (THD) within the output voltage, higher efficiency, lower standing voltage upon the power switches and low electromagnetic interference (EMI) [4–5]. In general, the multilevel inverter state is classified into three main groups: diode clamped, flying capacitor and cascaded multilevel inverter. There will not be capacitors voltage balancing problem or clamping diodes in cascaded multilevel inverters. Uniformity and modular structure of cascaded multilevel inverters has made it attractive in case of industry, although each unit cascaded multilevel inverter contains a DC source. The main problem of applying multilevel inverters

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is numerous power switches that normally contribute to the complexity and power switches management and a high cost. Each switch requires a related gate driver circuit. This may cause the overall system some expenses and complexities. Hence, the implementation, reducing the switching times, gate driver circuits and DC sources should be taken into account.

Novel topologies of cascaded multilevel inverter with reduced switches have been presented in [6] and [7]. It should be noticed that the presented topologies [6] and [7] need four high rating switches for the output side H-bridge. In other words, these topologies do not imply the main advantage of multilevel inverters. In [8], a recent cascaded multilevel inverter topology has been presented which considers applying a level doubling network (LDN). The LDN changes to a half-bridge inverter to double the output voltage level numbers. The rising problem here is the capacitor voltage balancing. In [9], the authors present a single-phase transformer less grid-connected photovoltaic converter based on two cascaded full bridges containing different DC-link voltages. Using a single DC bus, the converter can synthesize up to nine voltage levels, since only a full bridge is supplied by a flying capacitor. The main problem of the topology would be the capacitor voltage balancing, especially in case of high currents. A novel converter structure based on cascade converter family is presented in [10]. The proposed multilevel converter has lower switching times. The mentioned topology requires various DC sources and switches which include a higher peak inverse voltage (PIV) compared to the other switches. A new solar power generation system, which is composed of DC/DC power converter and a new seven-level inverter, presented in [11]. Applying a capacitor selection circuit and a full-bridge power converter would aid us figuring the novel 7-level inverter, which is connected to the cascade. The inverter is an asymmetric one. In [12] the proposed photovoltaic system is considered to have a single-phase seven-level inverter. This 7-level inverter contains six power switches. However, three dc capacitors are applied to construct three voltage levels, which results in a more balanced capacitor voltage being rather complex. In [13], a novel single-phase wind energy inverter (WEI) with a flexible AC transmission system (FACTS) capability is presented. In [14] a 5-level inverter is generated and applied to inject the actual power of the renewable power within the grid. Two DC capacitors, a dual-buck converter, a full-bridge inverter, and a filter configure the 5-level inverter. This 5-level inverter includes six power switches.

The article proposes a novel topology for cascaded multilevel inverters which generates vast levels with a low number of power switches and dc sources. The proposed converter operates as a symmetric and asymmetric converter. One procedure to calculate required magnitudes of DC voltage sources is proposed in asymmetric state. The proposed converter is based on the combination of developed H-bridge and half bridge inverters. A comparative analysis with some recently presented topologies and conventional structures is also provided. Finally, the experimental results are carried out to prove the feasibility of the proposed multilevel inverter. As the fastest growing renewable energy source, solar PV has gained great public attention in the past decade and is stepping into the main stream energy market. In this work, the multilevel inverter equipped with isolated DC/DC converters for PV–battery system is investigated.

2. Analysis of the proposed converter

The circuit of the proposed multilevel inverter is shown in Fig. 1. Proposed multi-level inverter, which is shown in Fig. 1 is composed of a developed H-bridge and series connection of half bridge inverter. As seen from Fig. 1, the half bridge inverter is comprised of two dc voltage sources and two switches. These half bridge inverters generate two levels. To avoid occurrence of short circuit on dc voltage sources, simultaneous conduction of switches must be avoided. The developed H-bridge is an inverter topology using an H-bridge output stage with a bidirectional auxiliary switch [15]. This inverter is used in the design of a 5-level inverter. As shown in Fig. 1, in any unit, each switch is consist of an MOSFET with an anti-parallel diode, except one switch. For example in first unit, only S1 is bi-directional switch and the other switches are unidirectional, from the blocking voltage viewpoint.

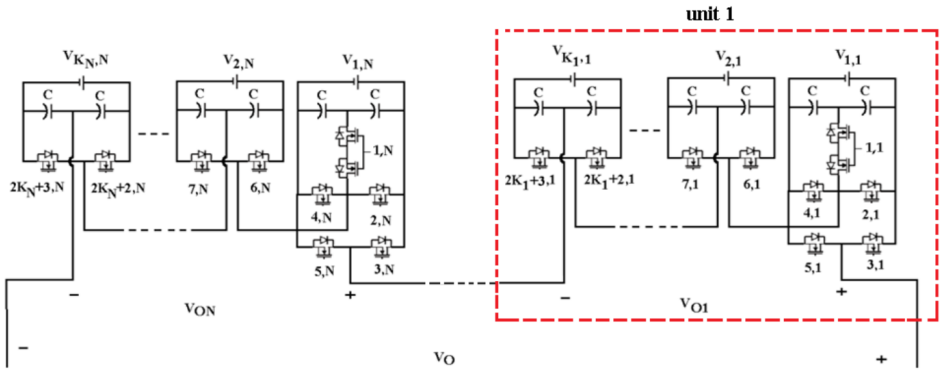

Fig. 1. Proposed multi-level inverter

The different unit generates a voltage wave form with a positive and negative polarity. The proposed topology constitutes of a series connection of inverters. The overall resulted voltage of the proposed cascaded multilevel inverter is configured by the sum of output voltages of the inverter units as follows:

$$V_{\mathrm{O}} = V_{\mathrm{O1}} + V_{\mathrm{O2}} + ... + V_{\mathrm{ON}}\,. \tag{1}$$

The different output voltage levels can be obtained by combinations of switching states of each unit. In the symmetric topology the magnitudes of all DC voltage sources are equal.

$$V_{1,1} = V_{2,1} = V_{K_1,1} = V_{2,1} = V_{2,2} = V_{K_2,2} = ... = V_{K_N,N} = V_{\mathrm{DC}}\,. \tag{2}$$

Considering the symmetric state, the number of output voltage levels N_{L} is calculated as

$$N_{\mathrm{L}} = \sum_{i=1}^{N}(2K_i + 3) - N + 1\,, \tag{3}$$

where K_i represents the number of dc voltage sources of the ith unit. The main objective in multilevel inverters design field is obtaining as many output voltage levels as least number of dc voltage sources and switches. Asymmetric topologies use DC sources with different magnitudes to maximize number of the generated voltage levels at the output for the same number of components, compared to the symmetrical topologies. To reduce the weight and size, an optimized structure must be obtained, so that considering the optimal structure to generate a given output voltage levels, there is less need to DC voltage sources and switches. One algorithm for determination of magnitudes of DC voltage sources is presented based on a binary algorithm. This algorithm can generate all voltage levels (odd and even) at the output of the multilevel inverter. In this algorithm, the base value of the per-unit systems considered is marked V_{DC}.

First unit:

$$V_{1,1} = V_{\mathrm{DC}}\,, \tag{4}$$

$$V_{j,1} = 2^{(j-1)} V_{\mathrm{DC}},\ j = 2, ..., K_1\,. \tag{5}$$

Second unit:

$$V_{1,2} = (1 + 4\sum_{j=1}^{K_1} V_{j,1}) V_{\mathrm{DC}}\,, \tag{6}$$

$$V_{j,2} = 2^{(j-1)} V_{1,2},\ j = 2, ..., K_2\,. \tag{7}$$

Nth unit:

$$V_{1,N} = (1 + 4\sum_{i=1}^{N-1}\sum_{j=1}^{K_i} V_{j,i}) V_{\mathrm{DC}}\,, \tag{8}$$

$$V_{j,N} = (2^{(j-1)}) V_{1,N},\ j = 2, ..., K_N\,. \tag{9}$$

According to this algorithm:

$$N_{\mathrm{L}} = \prod_{i=1}^{N} (2^{K_i+1} + 1) = (2^{K_1+1} + 1)(2^{K_2+1} + 1), ..., (2^{K_N+1} + 1)\,. \tag{10}$$

Suppose that the proposed topology consists of N sub-multilevel inverters and each of units has K_i DC voltage sources, $i = 1, 2, \ldots, N$. In that case, the number of switches in proposed topology is obtained as follows:

$$N_{\mathrm{sw}} = \sum_{i=1}^{N} (2K_i + 3) = 2(K_1 + K_2 + ... + K_N) + 3N\,. \tag{11}$$

Considering the number of DC voltage sources of different units as equal, then

$$K_1 = K_2 = ... = K_N = K\,, \tag{12}$$

$$N_{\rm sw} = (2K + 3)N\,, \tag{13}$$

$$N = \frac{N_{\rm sw}}{(2K + 3)}\,, \tag{14}$$

where K and N are the number of DC source in one unit and number of units, respectively. The maximum number of voltage levels for each two algorithms achieve from these following equations, respectively:

$$N_{\rm L} = 2(K + 1)N + 1 \text{ Symmetric state}\,, \tag{15}$$

$$N_{\rm L} = (2^{K+1} + 1)^N \text{ Asymmetric state}\,. \tag{16}$$

Grid and load-connected PV systems are a common and good proven due to their portions to renewable energy generation. The sight of PV systems is to elicit the maximum power from PV arrays and exalting the efficiency. Figure 2 shows hybrid power source to create DC-link of inverter. In this topology, several DC-DC converters, each of which is connected to a PV array and battery, share a single DC-link as an output. This topology presents several advantages such as: easy extension, independent maximum power tracking for each PV array and simple control schemes. Each hybrid power source is connected to the DC link of a specified cell of the multilevel inverter. PV arrays provide the main power, and the battery modules which accommodate the fast transients in power demands and guarantee the power quality and reliability of the hybrid power source. The bidirectional converter of the battery unit regulates the output voltages of the units at the desired values. Moreover, the bidirectional power flow of the battery module increases power management flexibility. The DC-DC converter of the PV unit is controlled such that the maximum power point tracking (MPPT) is achieved. The high frequency (HF) transformers increase voltage and create galvanic isolation. The voltage gain of DC-DC converter is:

$$V_{\rm O} = \frac{nD}{1 - D} V_1\,, \tag{17}$$

where n is the transformer ratio and D is the duty cycle of power semiconductor switch.

2.1. Ratings of semiconductors

The ratings of switches is considered to be an influential problem in multilevel inverters. The voltage and current ratings of the switches in an would influence the cost and realization. The currents of all switches are equal with the rated current

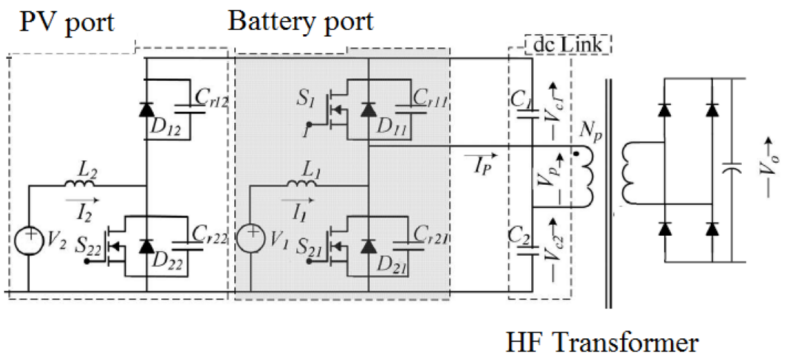

Fig. 2. Presented structure of the hybrid power source

of the load, in case of cascaded topologies. The PIV on unidirectional switches are given as

$$\mathrm{PIV}(i,j) = V_{i,j}\,. \tag{18}$$

To calculate the bidirectional switch PIV ,the dc voltage cell source must be divided by two.

2.2. Power loss calculation

Generally power electronic converters have losses. Refers to the given descriptions, the conduction and switching losses are commonly two kinds of losses. In the following expression (20) and (21) the instantaneous conduction losses of switches and diode are separately formulated [16]. Conduction losses are due to the equivalent resistance and the on-state voltage drop of the switches [16].

$$\rho_{\mathrm{c,T}}(t) = [V_{\mathrm{T}} + R_{\mathrm{T}} i^{\alpha}(t)]i(t)\,, \tag{19}$$

$$\rho_{\mathrm{c,D}}(t) = [V_{\mathrm{D}} + R_{\mathrm{D}} i(t)]i(t)\,, \tag{20}$$

where $\rho_{\mathrm{c,T}}(t)$ and $\rho_{\mathrm{c,D}}(t)$ denote the instantaneous conduction of the transistor device loss and diode, respectively, V_{T} and V_{D} are the ON-state voltage drops, while R_{T} and R_{D} are the equivalent on-state transistor device and diode resistances, respectively, and α is a constant manipulated by the transistor characteristics [16]. If K and N are considered to be the numbers of DC sources of each unit and unit numbers, then the number of turned on switches to generate one voltage level would be:

$$N_{\mathrm{on,sw}} = N(K+1)\,. \tag{21}$$

In other words, always, in each phase leg, a set of $N(K+1)$ switches is on at any given time so proposed inverter has less on-state voltage drop and conduction losses of switches.

The switching losses are because of nonideal operation of switches. The switching

losses are calculated for a typical switch and then the results are developed for the proposed multilevel converter:

$$p_{\mathrm{sw,T}} = [E_{\mathrm{on,T}} + E_{\mathrm{off,T}}] f_{\mathrm{sw}} \,, \tag{22}$$

$$p_{\mathrm{sw,D}} \cong E_{\mathrm{on,D}} f_{\mathrm{sw}} \,, \tag{23}$$

where p_{sw} denotes the switching power losses, E stands for the energy losses and f_{sw} is the switching frequency. Finally total switching power losses of a switch can be calculated as

$$p_{\mathrm{sw}} = p_{\mathrm{sw,T}} + p_{\mathrm{sw,D}} \,. \tag{24}$$

2.3. Comparison study

To probe the advantages and drawbacks of the proposed topology, it is compared to some previously presented novel topologies and the cascaded H-bridge inverter. The proposed symmetric topology is compared to symmetric structures and the proposed asymmetric topology is compared to the asymmetric ones. These comparisons are studied from the viewpoints of switching numbers, output voltage levels, driver circuits, dc voltage sources, variety of the dc voltage magnitudes, and the blocked voltages on switches. In recent years numerous topologies have been proposed in the article, but from components count minimization and number of level extending point of view, the topologies in [17] and [3] are novel ones which are selected for the mentioned comparison. Table 1 shows brief descriptions of selected topologies [17], [3], plus the cascaded H-bridge inverter. The binary asymmetric cascaded H-bridge inverter has been determined to the mentioned comparison in Table 1. In this Table, n is supposed to be the DC voltage source. Table 2 describes the proposed topology at two steps.

Table 1. Descriptions of selected topologies for comparison

Parameter	Inverter					
	Cascaded H-bridge		Topology of [17]		Topology of [3]	
	symm.	asymm.	symm.	asymm.	symm.	asymm.
Number of levels	$2n+1$	$2^{n+1}-1$	$2n+1$	$2^{n+1}-1$	$2n+1$	$3n+1$
Number of switches	$4n$	$4n$	$2n+2$	$2n+4$	$2n+4$	$2n+4$

The proposed structure has only one unit which consists of K DC voltage sources. In the second state the proposed structure has N units each of which consisting a dc voltage source. Table 3 summarizes the number of levels, switches, and DC sources at different steps of the proposed multilevel converter. If all of which have an equal number of cells, then $K_1 = K_2 = \cdots = K_N = K$.

Table 2. Descriptions of proposed topology for comparison

Parameter	Inverter			
	State 1 ($N = 1$, $K = n$		State 2 ($N = n$, $K = 1$	
	symmetric	asymmetric	symmetric	asymmetric
Number of levels	$4n + 1$	$2^{n+1} + 1$	$4n + 1$	5^n
Number of switches	$2n + 3$	$2n + 3$	$5n$	$5n$

Table 3. Proposed multilevel converter and its parameters.

Unit number	Cell number	Number of levels		Switches number	DC sources number
		symmetric	asymmetric		
$N = 1$	$K = 1$	5	5	5	1
	$K = 2$	7	9	7	2
	$K = 3$	9	17	9	3
	$K = 4$	11	33	11	4
	$K = 5$	13	65	13	5
$N = 2$	$K = 1$	9	25	10	2
	$K = 2$	13	81	14	4
	$K = 3$	17	289	18	6
	$K = 4$	21	1089	22	8
	$K = 5$	25	4225	26	10
$N = 3$	$K = 1$	13	125	15	3
	$K = 2$	19	729	19	6
	$K = 3$	25	4913	23	9
	$K = 4$	31	35937	27	12
	$K = 5$	37	274625	31	15

It can be inferred from Tables 1–3 that the proposed topology generates maximum levels each given number of switches, compared to the [17], [3] and cascaded H-bridge structures.

Figure 3 compares the proposed symmetric and selected topologies. Figure 3 shows that the proposed symmetrical topology generates higher number of levels per given number of switches, compared to the [17]and [3] structures specially only if $N = 1$ (state 1). Figure 4 shows the number of generated output voltage levels versus the number of switches at the asymmetric state. From Fig. 4, it is obvious that for a given number of switches, the proposed asymmetrical topology generate maximum number of levels compared to [17] and [3].

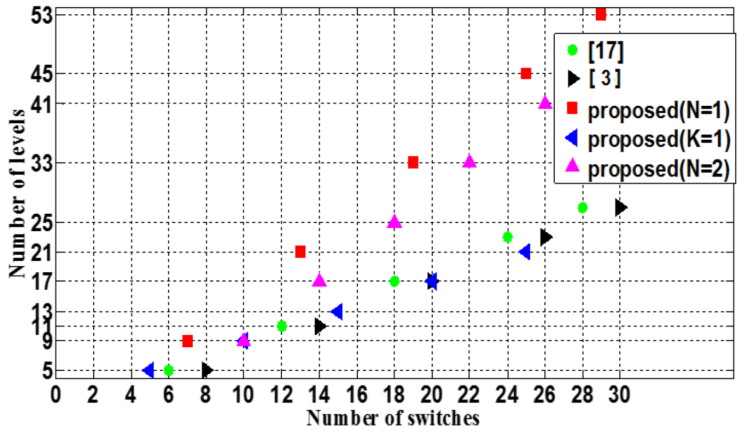

Fig. 3. Comparison between proposed structure and selected topologies in symmetric state

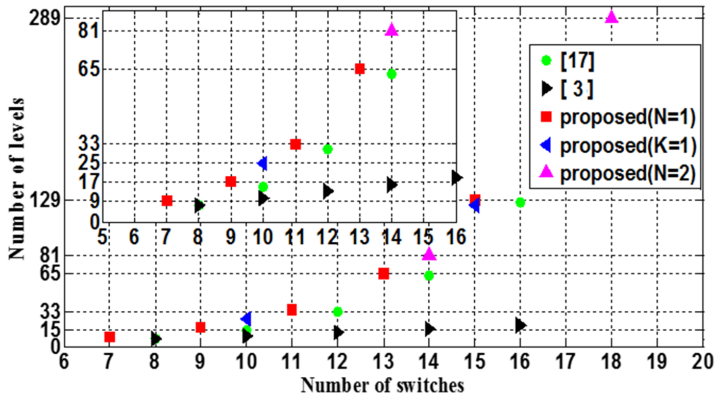

Fig. 4. Comparison between proposed structure and selected topologies in asymmetric state

3. Experimental results

To validate the maximum function of the proposed symmetrical and asymmetrical topologies, laboratory prototypes of symmetrical 9-level and asymmetrical 17-level inverters are applied. Figure 5 shows the circuit of laboratory prototypes of the mentioned inverter. In these circuits, IRFP460 MOSFET are applied as switching devices and IRS2113 driver circuits. To infer all switching algorithms, AVR microcontroller made by ATMEL Company has been applied. The capacitor is 4700 µF and load is a series R-L swith magnitudes 50 Ω and 150 mH, respectively.

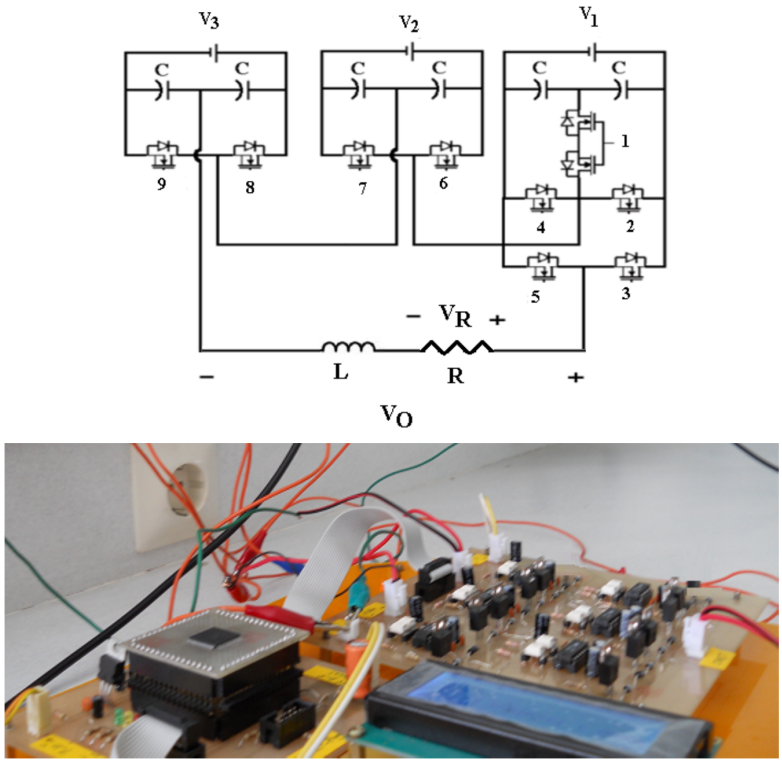

Fig. 5. Circuit of the hardware prototype

3.1. Symmetric state

The magnitude of each voltage sources of a symmetric case is considered 50 V ($V1 = V2 = V3 = 50$ V). Table 4 presents the ON switches lookup table of the single phase 9-level proposed converter and their corresponding levels. In each phase leg, a set of four switches is on at any given time. This structure generates nine voltage levels in each output phase as shown in Fig. 6.

Table 4. Look-up table of a single-phase 9-level converter

Level	ON switches	Level	ON switches
0	2,3,6,9	0	4,5,7,8
1	1,3,6,9	-1	1,5,7,8
2	3,4,6,9	-2	2,5,7,8
3	1,3,6,8	-3	1,5,7,9
4	3,4,6,8	-4	2,5,7,9

3.2. Asymmetric state

In case of asymmetric phase, the magnitude of voltage sources is considered as $V_1 = 25\,\mathrm{V}$, $V_2 = 50\,\mathrm{V}$ and $V_3 = 100\,\mathrm{V}$. Table 5 presents the ON switches lookup table of the single phase 17-level proposed converter and their corresponding levels. This structure generates seventeen voltage levels in each output phase as shown in Fig. 7.

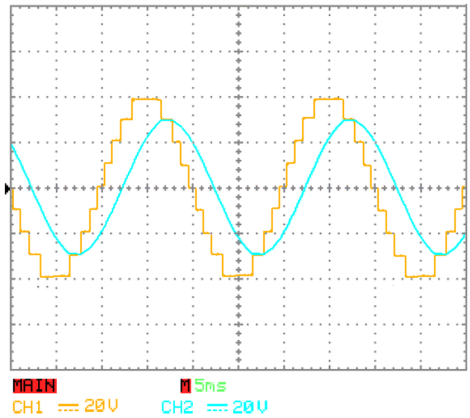

Fig. 6. Measured output voltage, and load resistance voltage (current)

Table 5. Look-up table of a single-phase 17-level converter

Level	ON switches	Level	ON switches
0	2,5,7,8	0	3,4,6,9
1	1,5,7,8	-1	1,3,6,9
2	2,3,7,8	-2	4,5,6,9
3	1,3,7,8	-3	1,5,6,9
4	3,4,7,8	-4	2,5,6,7
5	1,5,6,8	-5	1,3,7,9
6	2,3,6,8	-6	4,5,7,9
7	1,3,6,8	-7	1,5,7,9
8	3,4,6,8	-8	2,5,7,9

4. Conclusion

A novel configuration of multilevel inverter has been proposed. To reduce the drawbacks of multilevel inverter, we propose a modified circuit configuration of the conventional cascaded H-bridge multilevel inverter. It is capable of reducing switching numbers compared to the prior approach. Different selection patterns for DC sources can be applied to the proposed structure but two algorithms are considered

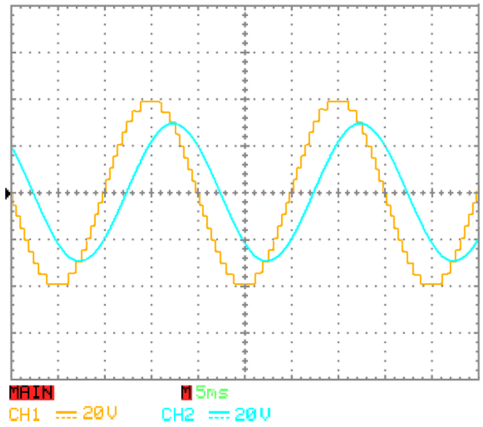

Fig. 7. Measured output voltage, and load resistance voltage (current)

and analyzed from the operating point of view. The operation and performance of the proposed converter has been verified on a prototype.

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